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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,668	12/19/2000	Akira Nonaka	09812.0497-00000	7062
22852	7590	01/30/2006	EXAMINER	
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP 901 NEW YORK AVENUE, NW WASHINGTON, DC 20001-4413			DAVIS, ZACHARY A	
		ART UNIT	PAPER NUMBER	
			2137	

DATE MAILED: 01/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/741,668	NONAKA ET AL.
	Examiner	Art Unit
	Zachary A. Davis	2137

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 04 November 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-11, 15-22 and 57 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-11, 15-22 and 57 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

1. An amendment was received on 04 November 2005. Claims 1, 17, and 57 have been amended. No claims have been added or canceled. Claims 1-11, 15-22, and 57 are currently pending in the present application.

Response to Arguments

2. Applicant's arguments filed 04 November 2005 have been fully considered but they are not persuasive.

Claim 57 was rejected under 35 U.S.C. 102(b) as anticipated by Christiano, US Patent 5671412. Claims 1-11 and 15-17 were rejected under 35 U.S.C. 103(a) as unpatentable over Schneier et al, US Patent 5768382, in view of Christiano. Claims 18-22 were rejected under 35 U.S.C. 103(a) as unpatentable over Schneier in view of Christiano and further in view of Castor et al, US Patent 5590288.

In reference to independent Claims 1, 17, and 57, Applicant argues that none of the cited references disclose a usage monitor that monitors usage control policy and status data to ensure that the content data is properly purchased and used based on a license. The Examiner respectfully disagrees. Although the relevant portion was not explicitly cited in the previous action, the Examiner believes that Christiano does disclose monitoring usage policy and status data to ensure that content is properly used based on a license (see column 6, line 60-column 7, line 46, where licenses are tracked

throughout the system; noting also column 10, lines 53-57). The Examiner further notes that, per Applicant's present disclosure, it appears that the usage monitor is not a physical structure, but instead a function performed by the arithmetic processing circuit or CPU (note Figures 68 and 69 where the physical hardware and connections are depicted, including CPU 1100, in contrast with Figure 30, depicting functional modules, including usage monitor 168; see also page 160, lines 8-11 of the present specification).

Further in reference to Claim 57, Applicant argues that "Nowhere in Christiano discloses a status data output, which later uses by the main processing unit to determine how the content data should be distributed to a user" (page 12 of the present response). The Examiner fails to appreciate this argument. Applicant additionally argues that Christiano does not disclose a status data containing content identification, a purchase mode, an identification for the circuit module, and a user identification, and that such information instead exists in a license request. However, the Examiner believes that the claimed "creating usage control status data" does not exclude a license request; the Examiner notes that the claim does not specify where or how the status data is created, and the Examiner further believes that the request for a license creates usage control status data in that the request for a license requests usage of the data and provides identification information (i.e. status data) to allow the request to be granted or denied based on a policy (column 10, lines 25-48). This is further supported by the description of the policies tracking licenses and usage data (column 6, line 60-column 7, line 46; column 10, lines 53-57). Further, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that

the features upon which applicant relies (i.e., "Christiano does not disclose the existence of such identification information in a status data generated by the arithmetic processing circuit as claimed", page 12 of the present response) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Specifically, Claim 57 makes no mention of status data generated by an arithmetic processing circuit, nor does the claim make any mention of an arithmetic processing unit whatsoever.

Therefore, for the reasons detailed above, the Examiner maintains the rejections as set forth below.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 57 is rejected under 35 U.S.C. 102(b) as being anticipated by Christiano, US Patent 5671412.

Christiano discloses a method including determining a usage or purchase mode based on a usage license policy (column 6, line 60-column 7, line 30); creating log data (column 18, lines 53-61); creating usage control status data (column 10, lines 53-57)

that includes a content identification (column 10, lines 27-33), the purchase mode (column 10, line 53-column 11, line 11), identification of a circuit module (column 10, lines 33-36), and a user identification (column 10, lines 53-57; column 6, lines 64-column 7, line 1; column 4, line 61-column 5, line 2); monitoring usage control policy and status data to ensure that content data is properly used based on a license (column 6, line 60-column 7, line 46; column 10, lines 53-57); controlling use of content data (column 10, line 64- column 11, line 3); recording the content data (column 10, lines 62-64, where the product is used on a computer system, and therefore stored at least temporarily therein; see also column 6, lines 28-31, where various storage media are disclosed); and encrypting key data and control data (column 14, lines 23-28).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-11 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneier et al, US Patent 5768382, in view of Christiano, US Patent 5671412.

In reference to Claim 1, Schneier discloses an apparatus within a tamper-resistant circuit module (column 8, lines 17-27; column 11, lines 31-37) including a first

bus (see Figures 4C-4H), an arithmetic processing circuit (Figure 4C, CPU 302), a storage circuit (Figure 4C, ROM 304), a second bus (see Figures 4C-4H), an interface circuit (see Figure 4C), an encryption processing circuit (Figure 4B-4C, encryption/decryption module 28; also column 11, lines 41-46), and an external bus interface circuit (Figure 4C, I/O 312). However, Schneier does not explicitly disclose determining a mode based on a handling policy and creating log data, nor does Schneier disclose creating usage control status data or controlling the use of the content data.

Christiano discloses determining a usage or purchase mode based on a usage license policy (column 6, line 60-column 7, line 30) and logging data (column 18, lines 53-61). Christiano further discloses creating usage control status data (column 10, lines 53-57) that includes a content identification (column 10, lines 27-33), the purchase mode (column 10, line 53-column 11, line 11), identification of a circuit module (column 10, lines 33-36), and a user identification (column 10, lines 53-57; column 6, lines 64-column 7, line 1; column 4, line 61-column 5, line 2). Christiano additionally discloses controlling use of content data (column 10, line 64- column 11, line 3) and a usage monitor that monitors the usage control policy and status data to ensure that content data is properly used based on a license (column 6, line 60-column 7, line 46; column 10, lines 53-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the apparatus of Schneier by including the usage policies and licensing as disclosed by Christiano, in order to provide a variety of

options and flexibility in controlling usage of licensed data (see Christiano, column 3, lines 12-19).

In reference to Claim 2, Schneier and Christiano further disclose a second interface circuit and that the first bus includes a third bus and a fourth bus (see Schneier, Figures 4C-4H).

In reference to Claim 3, Schneier and Christiano further disclose a third interface circuit communicating with a recording medium (see Schneier, Figure 4H, interface circuitry 406), a fifth bus, and a fourth interface circuit (see Schneier, Figures 4C-4H).

In reference to Claim 4, Schneier and Christiano further disclose a public key encryption circuit (see Schneier, column 10, lines 27-56) and a common key encryption circuit (see Schneier, column 9, line 62-column 10, line 11).

In reference to Claim 5, Schneier and Christiano further disclose that the storage circuit stores private and public key data (see Schneier, column 11, lines 44-48), the public key encryption circuit verifies the integrity of signature data and creates signature data (see Schneier, column 10, lines 41-56), and the common key encryption circuit encrypts and decrypts content data and key data using a session key (Schneier, column 9, line 65-column 10, line 6).

In reference to Claim 6, Schneier and Christiano further disclose a hash value generating circuit used by the public key encryption circuit in verifying and creating signatures (see Schneier, column 17, lines 46-50).

In reference to Claim 7, Schneier and Christiano further disclose a random number generating circuit (see Schneier, column 10, lines 57-67).

In reference to Claim 8, Schneier and Christiano further disclose an external storage circuit (see Schneier, column 7, lines 57-60).

In reference to Claims 9 and 11, Schneier and Christiano disclose everything as applied to Claim 8 above. Schneier and Christiano further disclose that programs are executed from memory in a conventional manner (see Schneier, column 7, lines 60-61). However, neither Schneier nor Christiano explicitly discloses a storage-circuit control circuit or a storage management circuit. Official notice is taken that it is well known in the computer arts to include a memory controller or memory management circuit, such as a DMA or MMU, in order to allow for the optimization of the use of memory. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the apparatus of Schneier and Christiano by including a memory controller or manager, in order to optimize the use of memory, as is well known in the computer arts.

In reference to Claim 10, Schneier and Christiano further disclose that the external bus is connected to a host processor (see Schneier, Figure 4C, where the I/O 312 is connected to external CPU 27).

In reference to Claim 15, Schneier and Christiano further disclose a real time clock (see Schneier, column 11, line 46). Further, Schneier and Christiano disclose encrypting key data and control data (see Christiano, column 14, lines 23-28) and storing license key data (Christiano, column 14, lines 19-21).

In reference to Claim 16, Schneier and Christiano further disclose that the storage circuit writes and erases data in units of blocks and also discloses a write lock

control circuit for controlling writing and erasing blocks of data (see Schneier, column 18, lines 39-43).

In reference to Claim 17, Schneier discloses an apparatus within a tamper-resistant circuit module (column 8, lines 17-27; column 11, lines 31-37) including a first bus (see Figures 4C-4H), an arithmetic processing circuit (Figure 4C, CPU 302), a storage circuit (Figure 4C, ROM 304), a second bus (see Figures 4C-4H), an interface circuit (see Figure 4C), an encryption processing circuit (Figure 4B-4C, encryption/decryption module 28; also column 11, lines 41-46), and an external bus interface circuit (Figure 4C, I/O 312). Schneier further discloses receiving an interrupt from an external circuit, performing processing, and reporting a result of the processing (column 11, lines 55-67). However, Schneier does not explicitly disclose determining a mode based on a handling policy and creating log data, nor does Schneier disclose creating usage control status data or controlling the use of the content data.

Christiano discloses determining a usage or purchase mode based on a usage license policy (column 6, line 60-column 7, line 30) and logging data (column 18, lines 53-61). Christiano further discloses creating usage control status data (column 10, lines 53-57) that includes a content identification (column 10, lines 27-33), the purchase mode (column 10, line 53-column 11, line 11), identification of a circuit module (column 10, lines 33-36), and a user identification (column 10, lines 53-57; column 6, lines 64-column 7, line 1; column 4, line 61-column 5, line 2). Christiano additionally discloses controlling use of content data (column 10, line 64- column 11, line 3) and a usage

monitor that monitors the usage control policy and status data to ensure that content data is properly used based on a license (column 6, line 60-column 7, line 46; column 10, lines 53-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the apparatus of Schneier by including the usage policies and licensing as disclosed by Christiano, in order to provide a variety of options and flexibility in controlling usage of licensed data (see Christiano, column 3, lines 12-19).

7. Claims 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneier in view of Christiano as applied to claim 17 above, and further in view of Castor et al, US Patent 5590288.

In reference to Claims 18 and 19, Schneier and Christiano disclose everything as applied to Claim 17 above. However, Schneier as modified above does not explicitly disclose reporting the result of processing by outputting an interrupt. Further, Schneier as modified above does not explicitly disclose that the external bus interface includes a common memory and that the external circuit obtains a result by polling.

Castor discloses a system which allows a computer to request another computer to execute a procedure (column 3, lines 38-42) including outputting an interrupt (column 12, lines 29-33). Castor further discloses a common memory (the buffer of column 12, lines 33-35) and polling an interface circuit to obtain a result (column 12, lines 35-47). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the apparatus of Schneier and Christiano by including the

interrupt, buffer, and polling of Castor, in order to increase reliability, lower cost, and allow easier upgrades in a distributed computing system (Castor, column 4, lines 11-21).

In reference to Claim 20, Schneier, Christiano, and Castor further disclose first status registers including flags (see Castor, column 12, lines 29-35).

In reference to Claim 21, Schneier, Christiano, and Castor further discloses storing and executing an interrupt program (see Castor, column 5, lines 49-51).

In reference to Claim 22, Schneier, Christiano, and Castor further discloses storing and executing a plurality of interrupt programs and subroutines (see Castor, column 5, lines 49-55).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zachary A. Davis whose telephone number is (571) 272-3870. The examiner can normally be reached on weekdays 8:30-6:00, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571) 272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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